Blind via capacitance

Brock J. LaMeres in his BSEE thesis for Montana State University [1] simulated (and corroborated with measurements) a number of simple 3-layer blind via configurations similar to figure 5.25.

The dielectric spacing between layer 1-2, and also layers 2-3, was 18.9 mils in all cases. The conductor thicknesses on layers 1, 2 and 3 were all the same (2.2 mils), yielding an overall via length of 44.4 mils. The values of capacitance should be treated as approximate. The capacitance for a shorter via would be considerably less.

Table 5.8—Blind-via capacitance (LaMeres)

Drilled hole dia., mil	Clearance dia., mil	Pad dia., mil	Via length, mil	Via capacitance C_V pF	Via inductance L_V pH
18	46	20	44	0.23	305
18	46	30	44	0.31	305
18	46	40	44	0.46	305
12	36	20	44	0.21	365
12	36	30	44	0.31	365
12	36	40	44	0.46	365
8	28	20	44	0.19	440
8	28	30	44	0.30	440
8	28	40	44	0.46	440

LaMeres reports that inductance of the via varies with the size of the drilled hole and the ground-plane clearance diameter, but not as a strong function of pad diameter. In all cases shown here the via impedance $\sqrt{L_V/C_V}$ remains less than 50 ohms, so the via appears essentially capacitive. The 8-mil hole with a 28-mil clearance and small 20-mil pad best approximates a 50-ohm through-connection.

The data in Table 5.8 may be extrapolated to other via sizes. If all the specifications for a via (drilled hole, pad, clearance, length, and inter-plane spacing) are scaled by a factor k, the capacitance and inductance of the resulting configuration also scale by the same factor k. The capacitance also scales in proportion to the dielectric constant of the pcb material. The dielectric constant of the substrate assumed in Table 5.8 is 4.3.

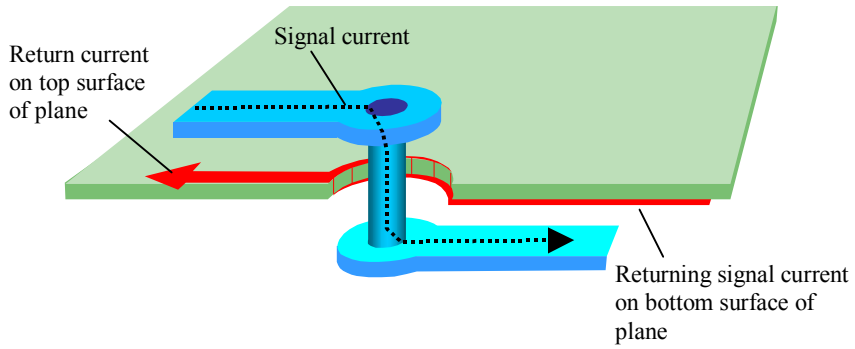

Figure 5.25—Returning signal current at a via pops between top and bottom surfaces of a solid reference plane by passing through the clearance hole.

Effect of back-drilling to remove excess length of PTH via

The total capacitance of a via depends on the properties of the via, the surrounding reference planes, and the dielectric constant of the substrate material. While the capacitance does depend on configuration of pads associated with the via, it does *not* depend on which pads are used to interconnect traces leading to and from the via.

For example, suppose in a 14-layer board a certain through-hole via accepts a signal coming in on layer 1 and leaving on layer 3. An identical adjacent via accepts a signal coming in on layer 1 and leaving on layer 14. Even though the signal current traverses different sections of the two vias, the voltages on the vias are the same in both cases, so the capacitances are the same. Central to this analysis, of course, is the assumption that the full length of the via is electrically short compared to the signal risetime.

In the event that your signal happens to traverse only layers 1 and 3, you might begin to wonder if it is possible to cut off the bottom section of the via (layers 4 through 14), thus reducing the capacitance. This is possible in three ways:

- The *blind-via process* drills and plates various sub-layers of a printed circuit board before final board lamination, making possible the existence of miniature vias penetrating only partway through the board stack.
- The *micro-via process* laser-ablates through only a very thin dielectric separating the outermost two layers of a printed-circuit board. The finished structure is equivalent to a blind-via process with holes only penetrating layers 1 and 2 (or the bottom-most two layers).
- Finished plated-through-hole (PTH) vias may be *back-drilled* after plating. This secondary process uses a drill bit slightly larger than the original drill bit used to form the via hole. The back-drilling bit penetrates from the backside of the board partway through. This process cuts away the metallized surface of the via wall from the backside of the board, leaving a conductive structure that penetrates from the top surface only partway through the board.

Table 5.9 lists the capacitances of typical through-hole vias that have been back-drilled, as reported by Teradyne [2]. These vias are used with press-fit connectors in very thick, high-speed backplanes with multiple solid reference planes. The total backplane thickness in these examples was 250 mils. The via length was modified by progressively back-drilling the via to shorten the plated length of the hole. Your results vary according to the configuration of reference planes within the board.

Table 5.9—PTH capacitance (Teradyne)

Drilled hole dia., mil	Plated hole dia., mil	Clearance dia., mil	Pad dia., mil	PTH length, mil	Via capacitance pF
26	22	52	38	250	2.4
26	22	52	38	200	2.0
26	22	52	38	225	1.8
26	22	52	38	150	1.5
26	22	52	38	125	1.3
26	22	52	38	100	1.0

The data in Table 5.9 may be extrapolated to other via sizes. If all the specifications for a via (drilled hole, pad, clearance, length, and inter-plane spacing) are scaled by a factor k, the capacitance of the resulting configuration also scales by the same factor k. The capacitance also scales in proportion to the dielectric constant of the pcb material. The dielectric constant of the substrate assumed in Table 5.9 is approximately four.

Example: Via capacitance

Assume your via dimensions are exactly half the values represented by row 5 of Table 5.9 (all values in mils):

13 drill

9 finished (irrelevant to electrical properties)
19 pad
26 clearance
63 length (use value of 125 in row 5 from table)

The capacitance listed in row 5 is 1.3 pF.
The capacitance of your scaled via is therefore estimated as 0.7 pF.

To more accurately estimate the capacitance of a via you should use a three-dimensional field solver.

References

[1] Brock J. LaMeres, *Characterization of a Printed Circuit Board Via*, B.S.E.E., Montana State University Technical Report EAS_ECE_2000_09, 1998, reprinted in part in *Microwave Journal*, November 2000, and later in *Conformity*, vol. 6, no. 7, July, 2001

[2] Teradyne, "Design Considerations for Gigabit Backplane Systems", IEC Web Proforum Tutorials, http://www.iec.org/online/tutorials/design_backplane/topic05.html