Short Transmission Line Examples

Source impedance:
ECL = 10 ohms
TTL/CMOS = 30 ohms

Lossless, distortionless transmission line

Unit
step

Load impedance
RL = 10K
CL = zero or 20 pF

IDEAL risetime = 6 x (line delay)

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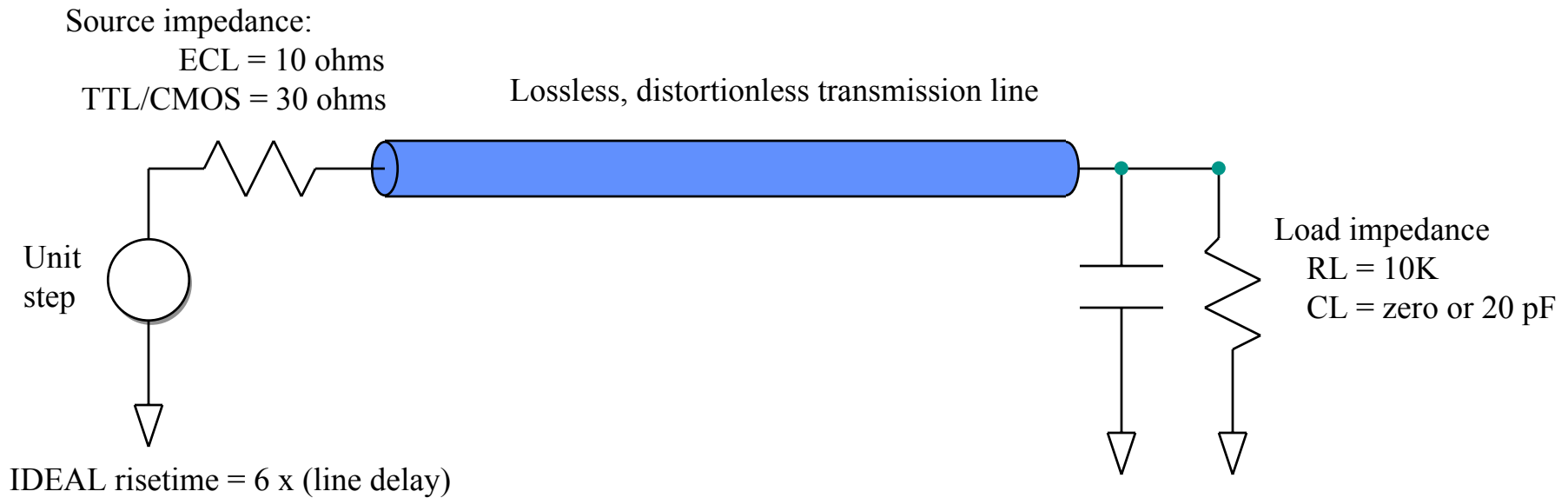
It's the Risetime/Delay Ratio that Counts

Set nominal transmission
line delay and risetime

$delay := 10^{-9}$ $ZS = 10$ $RL = 1 \cdot 10^4$

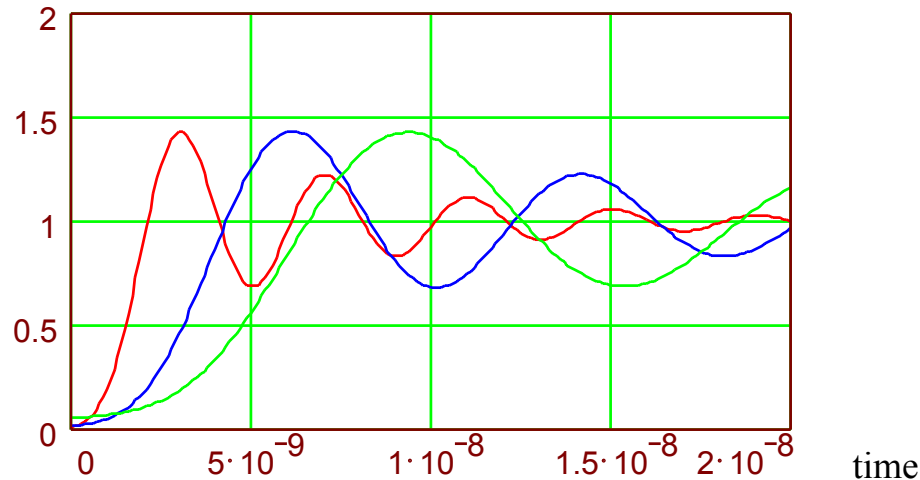$risetime := 2 \cdot delay$ $ZC = 65$ $CL = 0$

Scale both delay and risetime to see
what happens

$X1 := SYS3(delay, risetime)$

$X2 := SYS3(delay \cdot 2, risetime \cdot 2)$

$X3 := SYS3(delay \cdot 3, risetime \cdot 3)$

time

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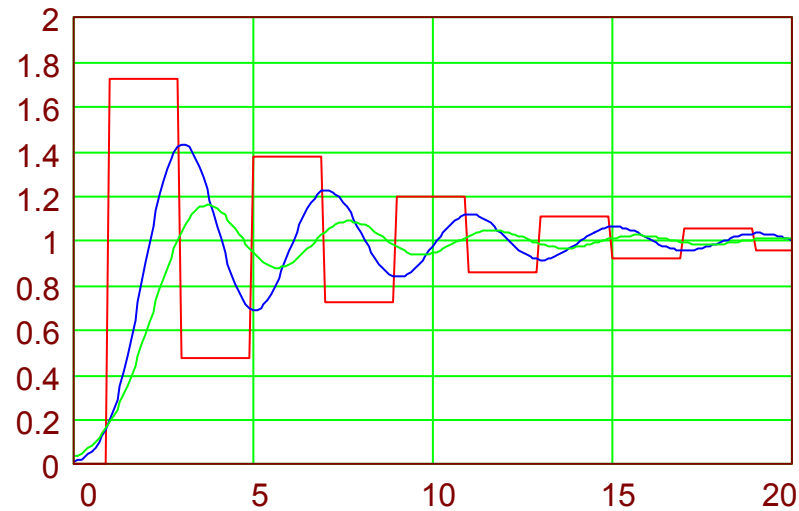# ECL

Unterminated line response
Risetime set to 0, 2 and 3 times transmission line delay

$ZS = 10$ $RL = 1 \cdot 10^4$
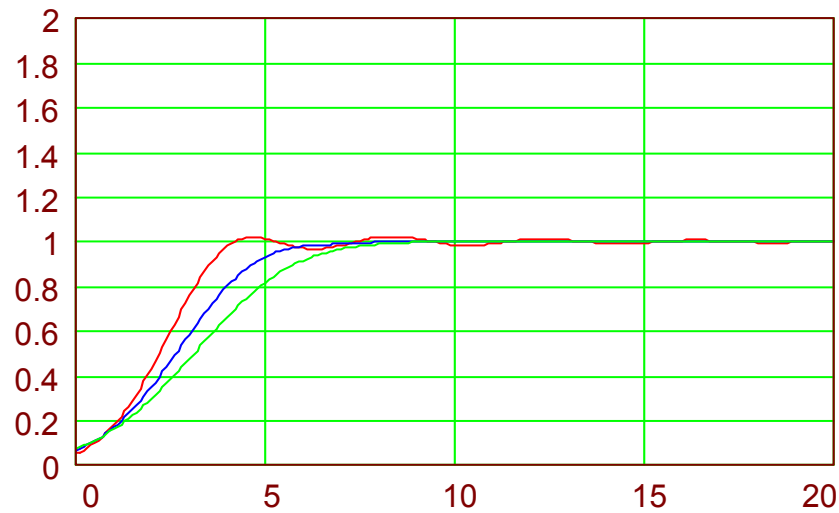
$ZC = 65$ $CL = 0$

time, in units
of line delay

ECL

Unterminated line response
Risetime set to 4, 5 and 6 times transmission line delay

ZS = 10 RL = $1 \cdot 10^4$

ZC = 65 CL = 0

time, in units
of line delay

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ECL
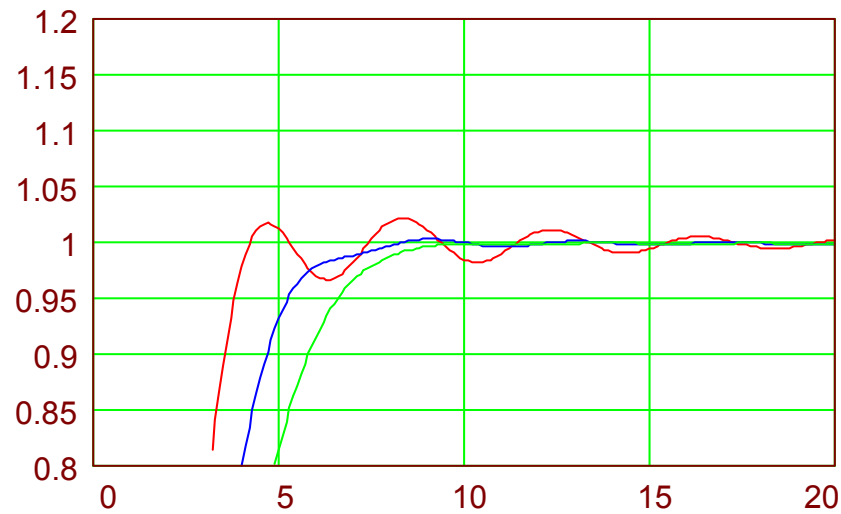
Unterminated line response
Risetime set to 4, 5 and 6 times transmission line delay
BLOWUP of vertical axis

$ZS = 10$ $RL = 1 \cdot 10^4$

$ZC = 65$ $CL = 0$

time, in units
of line delay
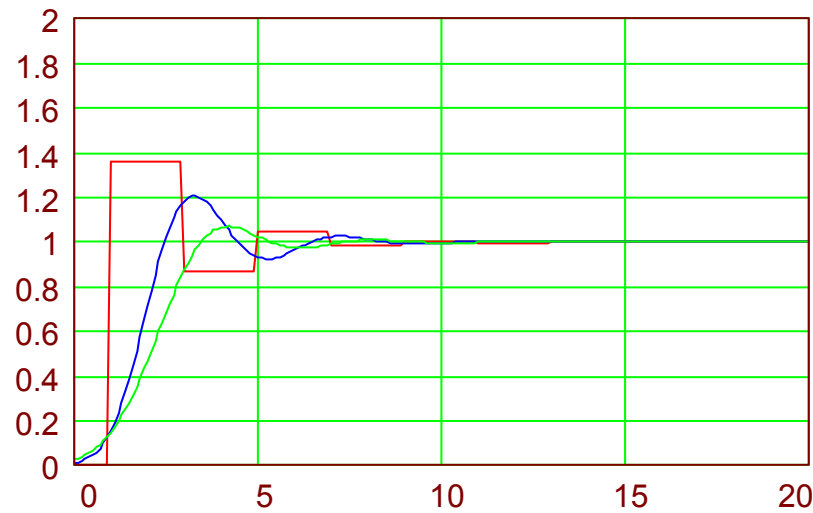
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TTL/CMOS

Unterminated line response
Risetime set to 0, 2 and 3 times transmission line delay

$ZS = 30$ $RL = 1 \cdot 10^{4}$

$ZC = 65$ $CL = 0$

time, in units
of line delay

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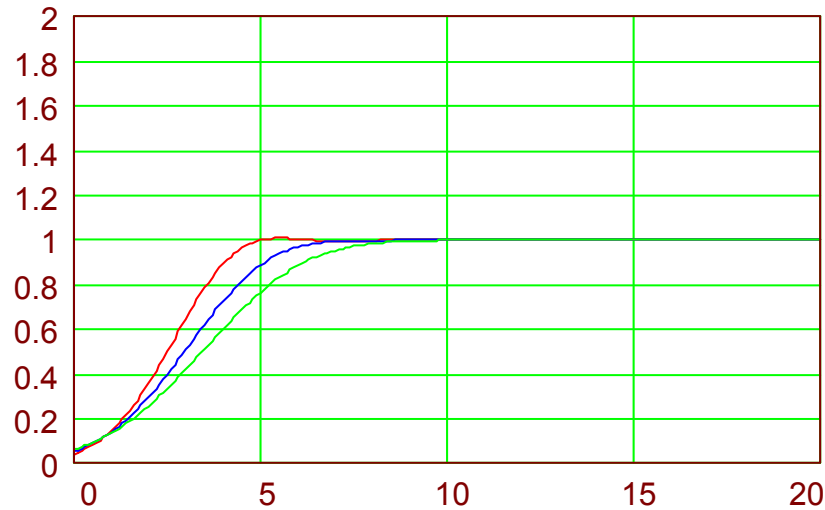# TTL/CMOS

Unterminated line response
Risetime set to 4, 5 and 6 times transmission line delay

$ZS = 30$ $RL = 1 \cdot 10^4$

$ZC = 65$ $CL = 0$

time, in units
of line delay

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TTL/CMOS

Unterminated line response
Risetime set to 4, 5 and 6 times transmission line delay
BLOWUP of vertical axis

$ZS = 30$ $RL = 1 \cdot 10^4$

$ZC = 65$ $CL = 0$

time, in units of line delay

High-Speed Digital Design
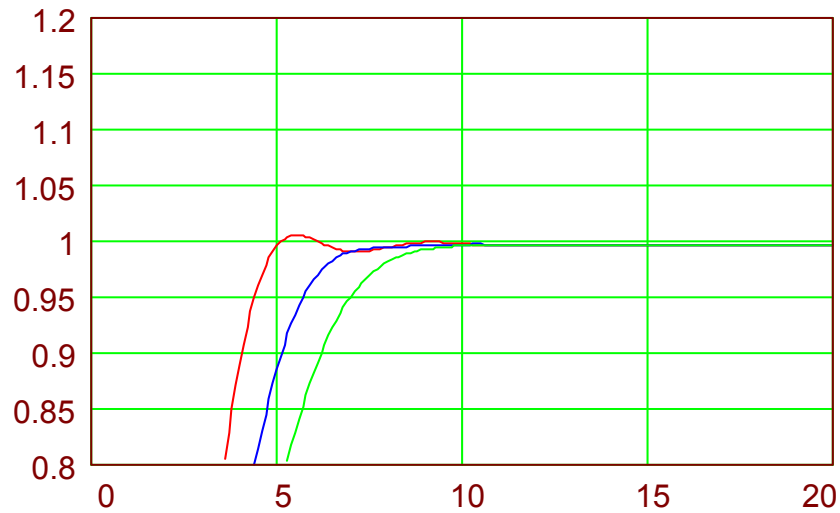
TTL/CMOS with Capacitive Load (20 pF)

Unterminated line response
Risetime set to 4, 5 and 6 times transmission line delay
BLOWUP of vertical axis
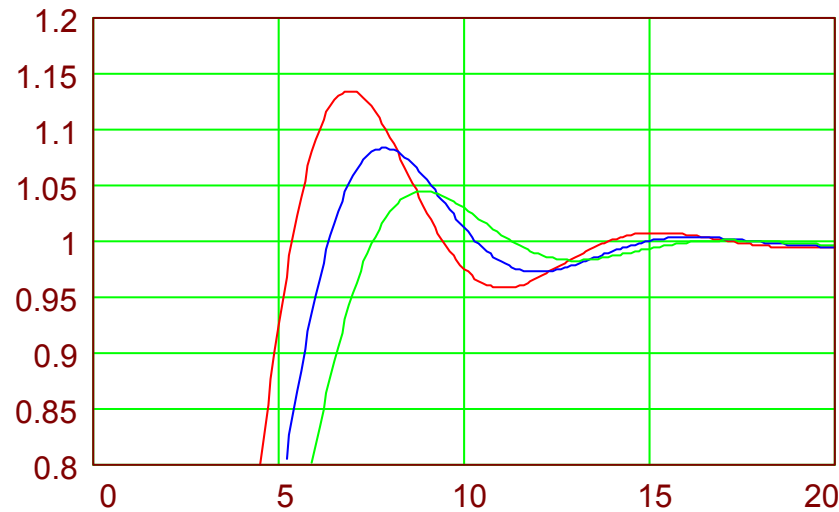
$$ZS = 30 \qquad RL = 1 \cdot 10^{4}$$

$$ZC = 65 \qquad CL = 2 \cdot 10^{-11}$$

time, in units
of line delay

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