



High-Speed Digital Design Seminar



Introduction to Black Magic, with
Dr. Howard Johnson

About this course

Printable Index

1. Vocabulary of Signal Integrity

High-Speed Digital Design: Opening Lecture.

HSDD Seminar (2015): 1.1-1.5.

[EE BASICS, MANAGEMENT] Definition of Signal Integrity. Relation to EMI. Purpose of Studying Signal Integrity. Overview of Program.

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Vocabulary. *HSDD Seminar (2015): 1.11-1.27.*

[CAPACITANCE, EE BASICS, INDUCTANCE] Your Schematic shows only the intended flow of signal power. Currents Form Loops. Every Loop of Current Has Inductance. Behavior of Inductance. Impedance Magnitude of Inductor. Effect of Inductor. Importance of Returning Current Path. Proximate Conductors Share Capacitance. How Capacitors Behave. Impedance Magnitude of Capacitor. Effect of Capacitor. Approximate Values of Capacitance. Practical Circuits are Littered with Parasitic Elements.

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Frequency Content of Digital Signals. *HSDD Seminar (2015): 1.28-1.41.*

HSDD Seminar (2015): 1.28-1.41.

[BANDWIDTH, EE BASICS, RINGING, RISE TIME] Data Band. Baud Interval Band (Rectangle = Step). Rising/Falling Edge Band. Frequencies That Matter for Digital Design. Meaning of

(pp. 28-41)

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"Frequency Response". Effect of Parasitics. Conceptual Frequency Response of Every PCB Trace. Relation of Knee Frequency to Circuit Performance. Effect of Shrinking Rise/Fall Time. International Technology Roadmap for Semiconductors (ITRS).

(25 min.) [Movie HD](#)

Effects of Delay. *HSDD Seminar (2015): 1.42-1.59.*
 [DELAY, LAYER STACK] Propagation Delay in Various Media. Example of Mixed Dielectric. Dielectric Properties of PCB Traces. Outer-Layer PCB Traces Are Faster. Distributed vs. Lumped Systems. Physical Length of Rising Edge. Pi Model of Transmission Line. Uses for The Pi Model.

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Lumped-Element Crosstalk. *HSDD Seminar (2015): 1.60-1.81.*
 [CAPACITANCE, CROSSTALK, INDUCTANCE] Step Response Theory. How Resistive Loading Changes Circuit Delay. Mutual Capacitance and Mutual Inductance. Measurement of Mutual Coupling. Comparison of Inductive and Capacitive Crosstalk. A Faraday Cage Fixes Capacitive Coupling. Mutual Inductance is a Current-Flow Problem. Improving the Return Path Fixes Inductive Crosstalk. Why Many Engineers Think First About Capacitance.

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Path of RF Current. *HSDD Seminar (2015): 1.82.*
 [INDUCTANCE, RETURNING SIGNAL CURRENT, SILAB HSDD] Experiments at 1 and 10 MHz demonstrate the effect of circuit layout on the flow of current.

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Skin and Dielectric Loss Chart. *HSDD Seminar (2015): 1.84-1.85.*
 [DIELECTRIC LOSS, SKIN EFFECT] Fibre Channel example at 1.06 Gb/s over 18 in. of FR-4 PCB trace.

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2. Properties of Gates

Properties of Gates. *HSDD Seminar (2015): 2.1-2.10.*
 [GROUND BOUNCE] Voltage Margin Budget. SSO Noise (Ground Bounce). SSO Test Setup. Theory of Operation. How SSO Noise Affects Inputs.

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Factors That Reduce Ground Bounce. *HSDD Seminar (2015): 2.8-2.17.*
 [DIFFERENTIAL SIGNALING, GROUND BOUNCE, POWER SYSTEMS, SPLIT

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PLANES] A Well-dispersed Array of Pwr/Gnd Pins. Differential Inputs. Shared Reference. Split-Power Architecture.

(10 min.) [Movie SD](#)

(10 min.) [Movie HD](#)

BGA Package Examples. *HSDD Seminar (2015): 2.18-2.21.*

[CHIP PACKAGING] Plastic Ball Grid Array (PBGA). Flip-Chip. Upside-down with heat spreader.

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IBIS I/O Buffer Information Specification. *HSDD Seminar (2015): 2.22-2.28.*

[SIMULATION] Live discussion of the purpose and appropriate use of modeling software.

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3. Using Your Oscilloscope

Scope Probes and Loading. *HSDD Seminar (2015): 3.1-3.9.*

[CAPACITANCE, PROBES] FET-input probe. Differential Active Probe. Resistive-input probe. Input Impedance of Probes. Effect of Probe on Signal Under Test. Which Probe is Best?

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Probe Rise Time and Bandwidth. *HSDD Seminar (2015): 3.10-3.13.*

[BANDWIDTH, PROBES] Combining Probe and Scope Bandwidths. Example Calculations.

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Probe Ground Wire. *HSDD Seminar (2015): 3.14-3.17.*

[INDUCTANCE, PROBES] Sensitivity to Length of Ground Wire. Using Short Ground Attachments.

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Spurious Magnetic Interference. *HSDD Seminar (2015): 3.18-3.25.*

[CROSSTALK, PROBES] Measuring Your Noise Floor. Probe Shield Currents. Differential Probing. Probing Without Ground.

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4. Transmission Lines

Transmission Lines. *HSDD Seminar (2015): 4.1-4.3.*
 [EE BASICS, TRANSMISSION LINE] What Makes a Transmission Line?.
 Four Main Properties.

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Characteristic Impedance. *HSDD Seminar (2015): 4.4-4.7.*

[CHARACTERISTIC IMPEDANCE, TRANSMISSION LINE] Response to Step
 Input. Ice-Cube Tray Analogy. Equivalence of Z₀ and RTERM.

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Example Geometries. *HSDD Seminar (2015): 4.8-4.10.*

[COAXIAL, LAYOUT, MICROSTRIP, STRIPLINE, TRANSMISSION LINE,
 TWISTED PAIR] Relations Between Impedance and Delay.

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Effects of Source and Load Impedance. *HSDD Seminar (2015): 4.11-4.17.*

[TERMINATION, TRANSMISSION LINE] Exponential Decay. Time-
 Space Diagram. Ways to Achieve Signal Convergence.

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Reflections. *HSDD Seminar (2015): 4.18-4.19.*

[REFLECTIONS, TRANSMISSION LINE] Reflection Function. Reflection
 Chart.

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Un-terminated Line Examples. *HSDD Seminar (2015): 4.20-4.30.*

[CIRCUIT TOPOLOGY, OVERSHOOT, RINGING, TRANSMISSION LINE]
 Example: Source Impedance Too Low. Example: Source
 Impedance Too High.

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Capacitive Loading of Transmission Line. *HSDD Seminar (2015): 4.31-4.34.*

[CAPACITANCE, CIRCUIT TOPOLOGY, RINGING, TRANSMISSION LINE]
 Tuned circuit analogy helps explain resonance.

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5. Solid Plane Layers

How Solid Plane Layers Control Crosstalk. *HSDD Seminar (2015): 5.1-5.10.*

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[CROSSTALK, REFERENCE PLANES, TRANSMISSION LINE] Early Computers vs. Multilayer PCB. Microstrip Response to Changing Magnetic Field. Magnetic Field Animations. Do Not Give Your PCB Vendor Full Control Over H and W. How Much Crosstalk Can You Take?. Where Simulation Fails Us.

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The Path of Returning Signal Current. *HSDD Seminar* (2015): 5.12-5.17.

Seminar (2015): 5.12-5.17.

[REFERENCE PLANES, RETURNING SIGNAL CURRENT, TRANSMISSION LINE] The High-Speed Path Can Look Pretty Strange. Distribution of High-Frequency Current Underneath a Signal Trace. What about Capacitance?. Crosstalk Versus Trace Separation Experiment. Crosstalk Over a Solid Ground Plane (waveforms). Crosstalk Over a Solid Ground Plane (graph).

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Stripline Crosstalk Study. *HSDD Seminar* (2015): 5.18-5.20.

[CROSSTALK, LAYOUT, STRIPLINE] Modeling crosstalk using the D/H ratio.

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Crosstalk is Directional. *HSDD Seminar* (2015): 5.21-5.23.

[CROSSTALK, MICROSTRIP, STRIPLINE, TRANSMISSION LINE] Classroom demonstration.

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Ground Plane Slots. *HSDD Seminar* (2015): 5.24-5.32.

[CROSSTALK, REFERENCE PLANES, RETURNING SIGNAL CURRENT, TRANSMISSION LINE] Traces Passing Over a Ground Plane Slot. Crosstalk From Ground Plane Slots. Connector Layout Slots. Crosstalk Versus Trace Separation Experiment. Crosstalk Over a Slotted Ground Plane (waveforms). Crosstalk Over a Slotted Ground Plane (graph). Why Wasn't the Lower Plane Very Effective?

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Multilayer Routing. *HSDD Seminar* (2015): 5.33-5.42.

[CROSSTALK, GUARD TRACE, LAYOUT] Power and Ground Fingers. Cross-Hatched Ground Grid. Guard Trace on a Two-Layer Board. Guard Trace on Multilayer Board (classroom demo covers slides 5.37 - 5.42).

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Split Power Planes. *HSDD Seminar* (2015): 5.43-5.46.

[CROSSTALK, LAYOUT, POWER SYSTEMS, SPLIT PLANES] Crossing a Split Power Plane Boundary. Use of Stitching Capacitors. Measuring Split-Plane Crosstalk.

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Layer Transitions. *HSDD Seminar* (2015): 5.47-5.49.

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[[LAYER STACK](#), [LAYOUT](#), [REFERENCE PLANES](#)] Implications for Fast Signals. Best Way to Route the Board.

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NASA Layer Stack. *HSDD Seminar (2015): 5.50-5.52.*

[[LAYER STACK](#), [LAYOUT](#), [REFERENCE PLANES](#)] Extemporaneous discussion of NASA layer stack.

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Segmenting the VCC Plane. *HSDD Seminar (2015): 5.53-5.54.*

[[LAYOUT](#), [POWER SYSTEMS](#), [SPLIT PLANES](#)] When to do it.

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Crosstalk NEXT and FEXT examples. *HSDD Seminar (2015): 5.55-5.66.*

[[CROSSTALK](#), [EXAMPLES](#)] Measuring NEXT and FEXT. Effect of trace length, height, and separation. Stripline FEXT. Effect of terminations..

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6. Terminations

Overview of Termination Types. *HSDD Seminar (2015): 6.1-6.3.*

[[RINGING](#), [TERMINATION](#), [TRANSMISSION LINE](#)] Systems that suffer ringing benefit from termination. Over-damped circuits do not.

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End Termination. *HSDD Seminar (2015): 6.4-6.15.*

[[CIRCUIT TOPOLOGY](#), [TERMINATION](#)] Function of Split Termination. Design Constraints. Thevenin Equivalent Model of End Termination. Design Process. Design Solution. Reflections from a Capacitive Load. Effect of Stub Hanging Beyond End Termination.

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Series Termination (Source Termination). *HSDD Seminar (2015): 6.16-6.27.*

[[CIRCUIT TOPOLOGY](#), [TERMINATION](#)] Halving and Doubling of Signal Amplitude. Value of External Series Resistor. No Clock Receivers Allowed in Middle of Series-Terminated Line. What's That Plateau?. What's That Glitch?. Heavy Capacitive Loads on Series and End-Terminated Lines. How Close Must a Series-Terminator Be to the Driver?

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Both-ends Termination. *HSDD Seminar (2015): 6.28.*

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[CIRCUIT TOPOLOGY, TERMINATION] The Ax-Murderer Approach to Termination.

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Comparison of Termination Styles. *HSDD Seminar (2015): 6.29-6.41.*

[CIRCUIT TOPOLOGY, EXAMPLES, TERMINATION] End Termination. Series Termination. AC Termination. Transmission Line States. Dynamic Termination. Proper Design of AC Termination. Power Dissipation. Comparison of Terminations (chart).

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Effect of Capacitive Loads. *HSDD Seminar (2015): 6.42-6.52.*

[CAPACITANCE, CIRCUIT TOPOLOGY, REFLECTIONS] Single Load in Middle of Line. Multiple Loads. Slowing Down the Rise Time. Adjusting the End Termination. Key Equations. Idea for Design.

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Source-Terminated Bus Structures. *HSDD Seminar (2015): 6.53-6.57.*

[MULTI DROP, TERMINATION, TRANSMISSION LINE] PCI-Bus (ver. 2.1, 1995). Compromises in Design. Circle Bus.

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Multiple Loads at End of Series-Terminated Line. *HSDD Seminar (2015): 6.59.*

[CAPACITANCE, TERMINATION, TRANSMISSION LINE] Effect on signal risetime.

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Bi-directional Termination. *HSDD Seminar (2015): 6.60.*

[CIRCUIT TOPOLOGY, MULTI DROP, TERMINATION] A uni-linear structure that can reverse direction.

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Risetime with Reactive Load. *HSDD Seminar (2015): 6.61-6.62.*

[CAPACITANCE, CIRCUIT TOPOLOGY, INDUCTANCE, RISE TIME] Capacitive load effect on risetime. Inductive bead effect on risetime.

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Diode Termination. *HSDD Seminar (2015): 6.63-6.64.*

[CIRCUIT TOPOLOGY, EXAMPLES, TERMINATION] Limitations of the approach. Examples.

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Weak End-Termination. *HSDD Seminar* (2015): 6.65.
 [CIRCUIT TOPOLOGY, TERMINATION] Terminations do not have to be perfect.

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End-Termination of Differential Signals. *HSDD Seminar* (2015): 6.66.

[CIRCUIT TOPOLOGY, DIFFERENTIAL SIGNALING, TERMINATION]
 Differential and common-mode termination concepts.

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Differential Termination with Re-Biasing. *HSDD Seminar* (2015): 6.67.

[CIRCUIT TOPOLOGY, DIFFERENTIAL SIGNALING, TERMINATION] Clever ways to change the DC offset of your differential signal.

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Tight Coupling. *HSDD Seminar* (2015): 6.68.

[DIFFERENTIAL SIGNALING, LAYOUT] Summary of effects (good and bad).

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Right-Angle Bends. *HSDD Seminar* (2015): 6.69-6.71.

[LAYOUT, REFLECTIONS, TRANSMISSION LINE] Common sense related to feature size and uniformity.

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Via Reflections. *HSDD Seminar* (2015): 6.72-6.73.

[LAYOUT, REFLECTIONS, TRANSMISSION LINE] Treating the via as a lumped capacitance. Effect of short trace stubs.

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Gigabit Ethernet Examples. *HSDD Seminar* (2015): 6.74-6.82.

[DIELECTRIC LOSS, DISPERSION, EXAMPLES, REFLECTIONS, SKIN EFFECT, TRANSMISSION LINE] Serial interface at 1.25 Gb/s. Showing dielectric loss and skin effect. Showing effect of vias and mismatched terminations. Showing effect of both-ends termination vs. single-end.

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7. Vias

Vias. *HSDD Book* (1993): Chap 7.

[VIAS] Chapter 7 from the book *High-Speed Digital Design: A Handbook of Black Magic* was not filmed.

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[Book](#)

8. Rock-Solid Power

Inductance of Bypass Capacitor. *HSDD Seminar* (2015): 8.1-8.13.

[BYPASS CAPACITORS, INDUCTANCE, LAYOUT, SILAB HSDD] Electrical performance model useful for capacitor types.

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Measured Data. *HSDD Seminar* (2015): 8.14-8.19.

[BYPASS CAPACITORS, EXAMPLES, INDUCTANCE, LAYOUT] Surface-Mounted Configurations. Inductance of Surface-Mounted Layouts (table). New Surface-Mounted Packages. AVX Interdigitated Capacitor (IDC).

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Arrays of Capacitors. *HSDD Seminar* (2015): 8.20-8.26.

[BYPASS CAPACITORS, POWER SYSTEMS] Modeling a Complete Power System. Dual-Value Capacitor Arrays. Choose the Smallest Package and the Biggest Value.

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HSDD Seminar—Extra Material

Metastability of a Flip-Flop. *HSDD Seminar* (2015).

[METASTABILITY, RELIABILITY, SILAB HSDD] Principle of metastability. When it matters. How to mitigate it.

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About This Course

High-Speed Digital Design covers the important and timely issues involving both high-speed digital design and signal integrity. Developed specifically for engineers and designers who work with high-speed digital signals, this workshop will give you the power to instantly recognize and solve many of today's high-speed design problems.

Main Topics

probes

crosstalk

ringing

chip packaging

[termination](#)[circuit topology](#)[reference planes](#)[returning signal current](#)[power systems](#)[bypass capacitors](#)

Who should watch this course?

- Digital logic designers
- System architects
- Chip designers
- EMC specialists
- Applications engineers
- Technicians
- Printed wiring layout professionals
- Managers and sales people in the high-speed digital industry
- Anyone who works with digital logic at high speeds (20MHz to 20GHz and beyond)

This is a practical two-day seminar course. It is filled with examples, explanations, and classroom demonstrations. Anyone who works with high-speed digital signals will understand and benefit from the material presented. It presents material related to the book, *High-Speed Digital Design: A Handbook of Black Magic*, but treated in a different way and with different examples. The book, being 447 pages in length, obviously delves into the subject matter in greater detail. Think of the seminar as an introduction and, if you like it, get the book for on-the-job reference.

[Go to the course](#)[Show me the book](#)

How to view this course

The author recommends that you view no more than one hour at a time. It may help for you to print out the notes pages for each lecture and take written notes. The sections in the notes marked *Points to Remember* are not often highlighted in the lecture, but offer good opportunities for personal thought and reflection.

The three courses provide a certain degree of redundancy. Each begins with a section designed to make each attendee aware of certain basic concepts and vocabulary peculiar to that course. Where there is overlap, the author emphasizes different aspects of the core material, uses different examples, and approaches the subjects from varying angles. He recommends that you watch all three courses, all the way through, including all the extra movies.

The course materials cover much more material than could possibly be presented in the six days of lecture that we were able to film. Dr. Johnson arranged the slides with extra material to give himself the flexibility to focus on specific issues of interest to each particular class and to respond to questions. We include the full set of student materials here for your reference, even though some of those slides were not filmed. To help you keep on track, slide numbers appear on the right side of the course contents listing.

In addition to the student course materials, the collection includes a full set of instructor materials in Powerpoint format. The instructor materials include original source artwork that may be of interest to those attempting to teach these courses. The necessary animation files, should you wish to use them independent of the lectures, are also available.

[Go to the course](#)[Get the animations](#)

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